Features

- Functionally and Pin Compatible with the Atmel Rad Hard AT40KAL Series
- Ultra High Performance
  - System Speeds to 85 MHz
  - Array Multipliers > 45 MHz
  - 14 ns Flexible SRAM
  - Internal Tri-state Capability in Each Cell
- FreeRAM™
  - Flexible, Single/Dual Port, Sync/Async 14 ns SRAM
  - 18432 Bits of Distributed SRAM Independent of Logic Cells for AT40KAL
- 384 PCI Compliant I/Os
  - Programmable Output Drive
  - Fast, Flexible Array Access Facilitates Pin Locking
- 8 Global Clocks
  - Fast, Low Skew Clock Distribution
  - Programmable Rising/Falling Edge Transitions
  - Distributed Clock Shutdown Capability for Low Power Management
  - Global Reset/Asynchronous Reset Options
  - 4 Additional Dedicated PCI Clocks
- Cache Logic® Dynamic Full/Partial Reconfigurability In-System
  - Unlimited Reprogrammability via Serial or Parallel Modes
  - Enables Adaptive Designs
  - Enables Fast Vector Multiplier Updates
  - Quick-Change™ Tools for Fast, Easy Design Changes
- Package Options
  - MQFPF160
- Industry-standard Design Tools
  - Seamless Integration (Libraries, Interface, Full Back-annotation) with Exemplar™, Mentor®, Synplicity®
  - Timing Driven Placement & Routing
  - Automatic/Interactive Multi-chip Partitioning
  - Fast, Efficient Synthesis
  - Over 75 Automatic Component Generators Create 1000s of Reusable, Fully Deterministic Logic and RAM Functions
- Intellectual Property Cores
  - Fir Filters, UARTs, PCI, FFT and Other System Level Functions
- Easy Migration to Atmel Gate Arrays for High Volume Production
- Supply Voltage 3.3V
- Design Tools
  - ATDH40M: Mother Board
  - ATDH40D160M: Daughter Board for MQFPF160
  - ATDS2100PC: IDS Software Design Kit
  - ATDH 2225: AT17 Series Configuration Memory ISP Downloadable
- QML Q Quality Grade

Military Reprogrammable FPGAs with FreeRAM™

AT40KAL

Preliminary

Rev. 4263B–AERO–06/03

Table 1. AT40KAL

Device	AT40KAL040
Usable Gates	40K - 50K
Rows x Columns	48 x 48
Cells	2,304
Registers	3,048(1)
RAM Bits	18,432
I/O (max)	384

Note: 1. Packages with FCK will have 8 less clocks.

Description

The AT40KAL is a family of fully PCI-compliant, SRAM-based FPGAs with distributed 14 ns programmable synchronous/asynchronous, dual port/single port SRAM, 8 global clocks, Cache Logic ability (partially or fully reconfigurable without loss of data), automatic component generators, and 50,000 usable gates. I/O counts range from 128 to 384 in Aerospace standard packages and support 3.3V.

The AT40KAL is designed to quickly implement high performance, large gate count designs through the use of synthesis and schematic-based tools used on a PC and Sun™ platform. Atmel's design tools provide seamless integration with industry standard tools such as Synplicity, Modelsim, Exemplar and Viewlogic. See the IDS datasheet for other supported tools.

The AT40KAL can be used as a co-processor for high-speed (DSP/processor-based) designs by implementing a variety of compute-intensive, arithmetic functions. These include adaptive finite impulse response (FIR) filters, Fast Fourier Transforms (FFT), convolvers, interpolators and discrete-cosine transforms (DCT) that are required for video compression and decompression, encryption, convolution and other multimedia applications.

Fast, Flexible and Efficient SRAM

The AT40KAL FPGA offers a patented distributed 11 - 13 ns SRAM capability where the RAM can be used without losing logic resources. Multiple independent, synchronous or asynchronous, dual port or single port RAM functions (FIFO, scratch pad, etc.) can be created using Atmel's macro generator tool.

Fast, Efficient Array and Vector Multipliers

The AT40KAL's patented 8-sided core cell with direct horizontal, vertical and diagonal cell-to-cell connections implements ultra fast array multipliers without using any busing resources. The AT40KAL's Cache Logic capability enables a large number of design coefficients and variables to be implemented in a very small amount of silicon, enabling vast improvement in system speed at much lower cost than conventional FPGAs.

Cache Logic Design

The AT40KAL is capable of implementing Cache Logic (Dynamic full/partial logic reconfiguration, without loss of data, on-the-fly) for building adaptive logic and systems. As new logic functions are required, they can be loaded into the logic cache without losing the data already there or disrupting the operation of the rest of the chip; replacing or complementing the active logic. The AT40KAL can act as a reconfigurable co-processor.

Automatic Component Generators

The AT40KAL FPGA family is capable of implementing user-defined, automatically generated, macros in multiple designs; speed and functionality are unaffected by the macro orientation or density of the target device. This enables the fastest, most predictable and efficient FPGA design approach and minimizes design risk by reusing already proven functions. The Automatic Component Generators work seamlessly with industry-stan-

dard schematic and synthesis tools to create the fastest, most efficient designs available.

The patented AT40KAL series architecture employs a symmetrical grid of small yet powerful cells connected to a flexible busing network. Independently controlled clocks and resets govern every column of cells. The array is surrounded by programmable I/O.

Devices offer 50,000 usable gates, and have 3,056 registers. AT40KAL series FPGAs utilize a reliable 0.35µ single-poly, 4-metal CMOS process and are 100% factory-tested. Atmel's PC- and workstation-based integrated development system (IDS) is used to create AT40KAL series designs. Multiple design entry methods are supported.

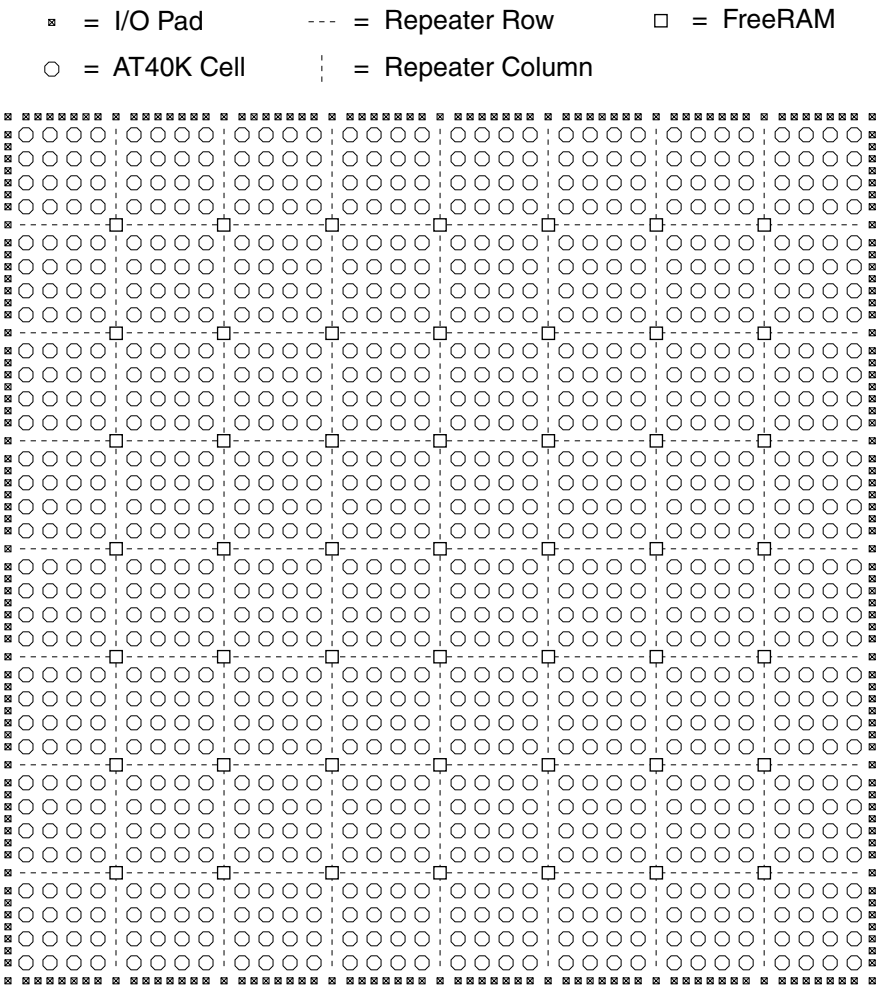
The Atmel architecture was developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, efficient and can implement any pair of Boolean functions of (the same) three inputs or any single Boolean function of four inputs. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances.

The Symmetrical Array

At the heart of the Atmel architecture is a symmetrical array of identical cells (Figure 1). The array is continuous from one edge to the other, except for bus repeaters spaced every four cells (Figure 2 on page 5). At the intersection of each repeater row and column is a 32 x 4 RAM block accessible by adjacent buses. The RAM can be configured as either a single-ported or dual-ported RAM[1], with either synchronous or asynchronous operation.

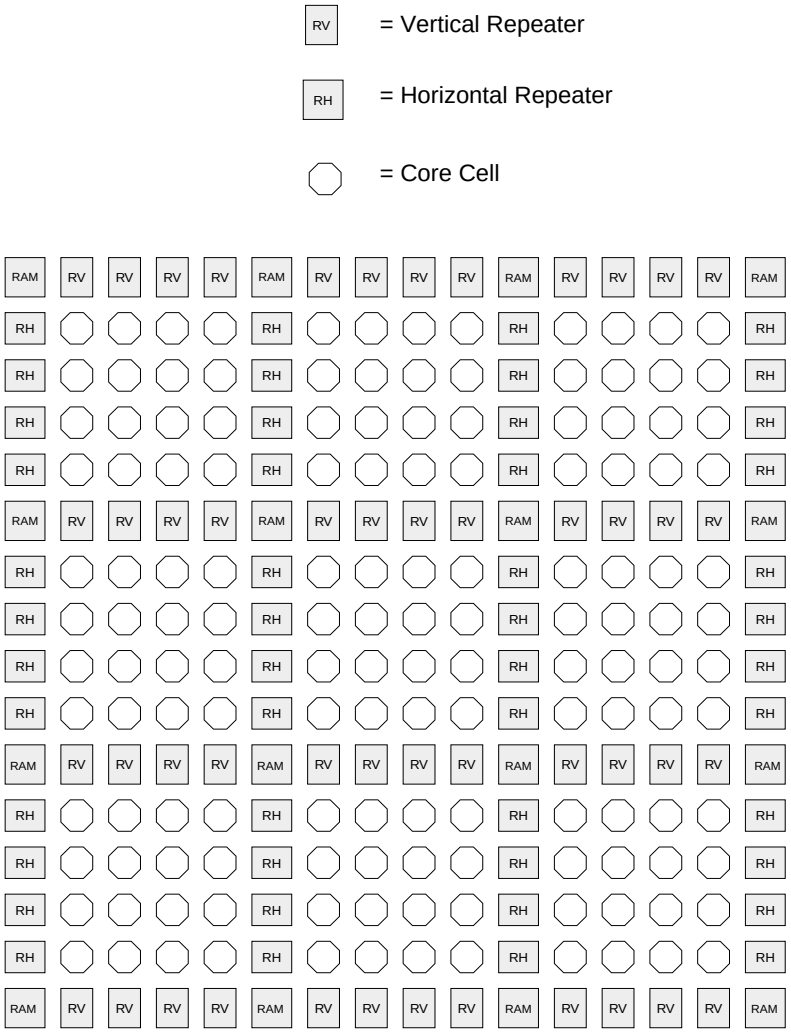
Note: 1. The right-most column can only be used as single-port RAM.

Figure 1. Symmetrical Array Surrounded by I/O (AT40K20)



Note: AT40KAL has registered I/Os. Group enable every sector for tri-states on obuf's.

Figure 2. Floorplan (Representative Portion)[1]



Note: 1. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. This is done automatically using the integrated development system (IDS) tool.

The Busing Network

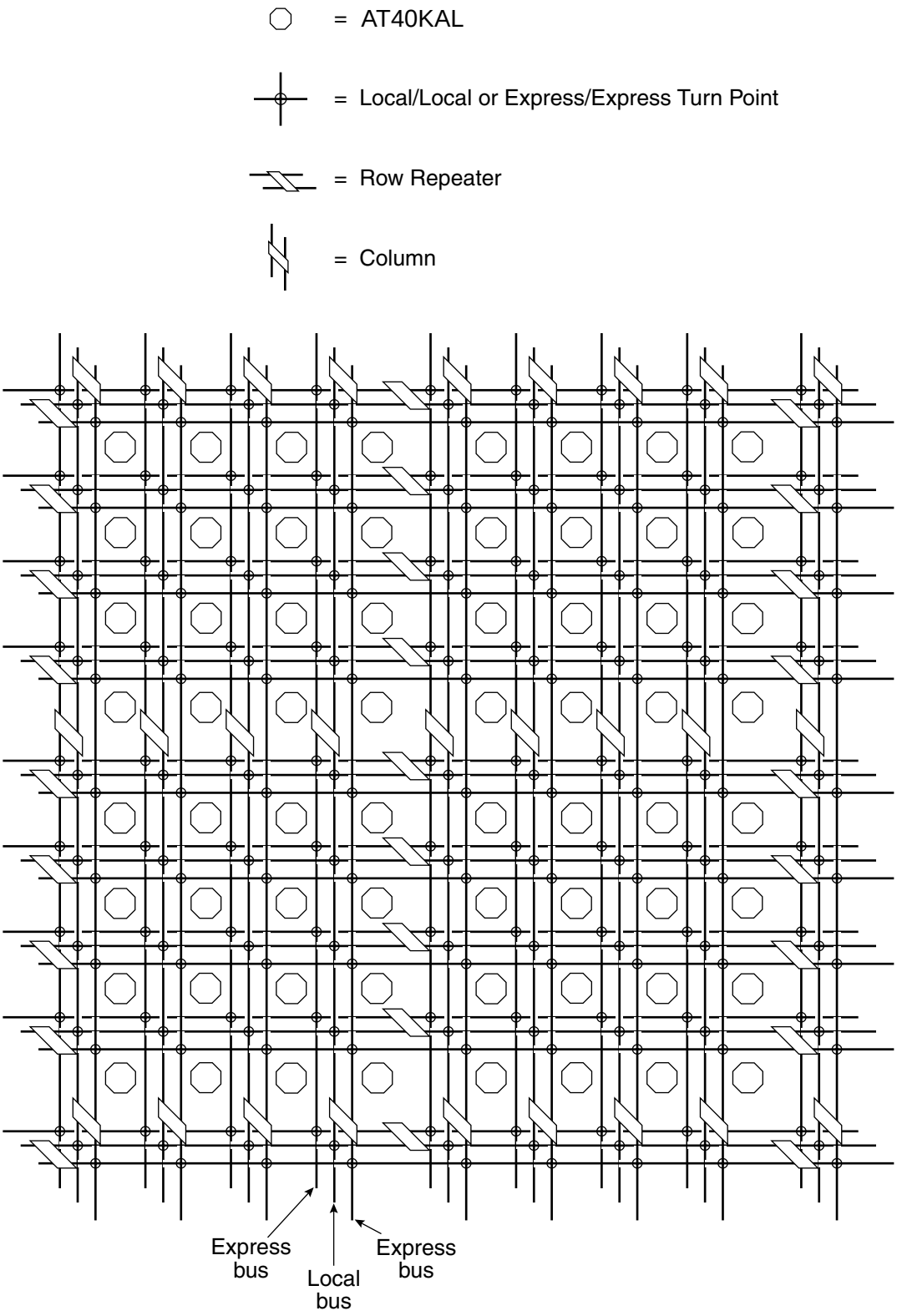
Figure 3 on page 7 depicts one of five identical busing planes. Each plane has three bus resources: a local-bus resource (the middle bus) and two express-bus (both sides) resources. Bus resources are connected via repeaters. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. Each local-bus segment spans four cells and connects to consecutive repeaters. Each express-bus segment spans eight cells and “leapfrogs” or bypasses a repeater. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Although not shown, a local bus can bypass a repeater via a programmable pass gate allowing long on-chip tri-state buses to be created. Local/Local turns are implemented through pass gates in the cell-bus interface (see following page). Express/Express turns are implemented through separate pass gates distributed throughout the array.

Some of the bus resource on the AT40KAL is used as a dual-function resource. Table 2 shows which buses are used in a dual-function mode and which bus plane is used. The AT40KAL software tools are designed to accommodate dual-function buses in an efficient manner.

Table 2. Dual-function Buses

Function	Type	Plane(s)	Direction	Comments
Cell Output Enable	Local	5	Horizontal and Vertical	
RAM Output Enable	Express	2	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Write Enable	Express	1	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Address	Express	1 - 5	Vertical	Buses full length at array edge Buses in second column to left of RAM block
RAM Data In	Local	1	Horizontal	
RAM Data Out	Local	2	Horizontal	
Clocking	Express	4	Vertical	Bus half length at array edge
Set/Reset	Express	5	Vertical	Bus half length at array edge

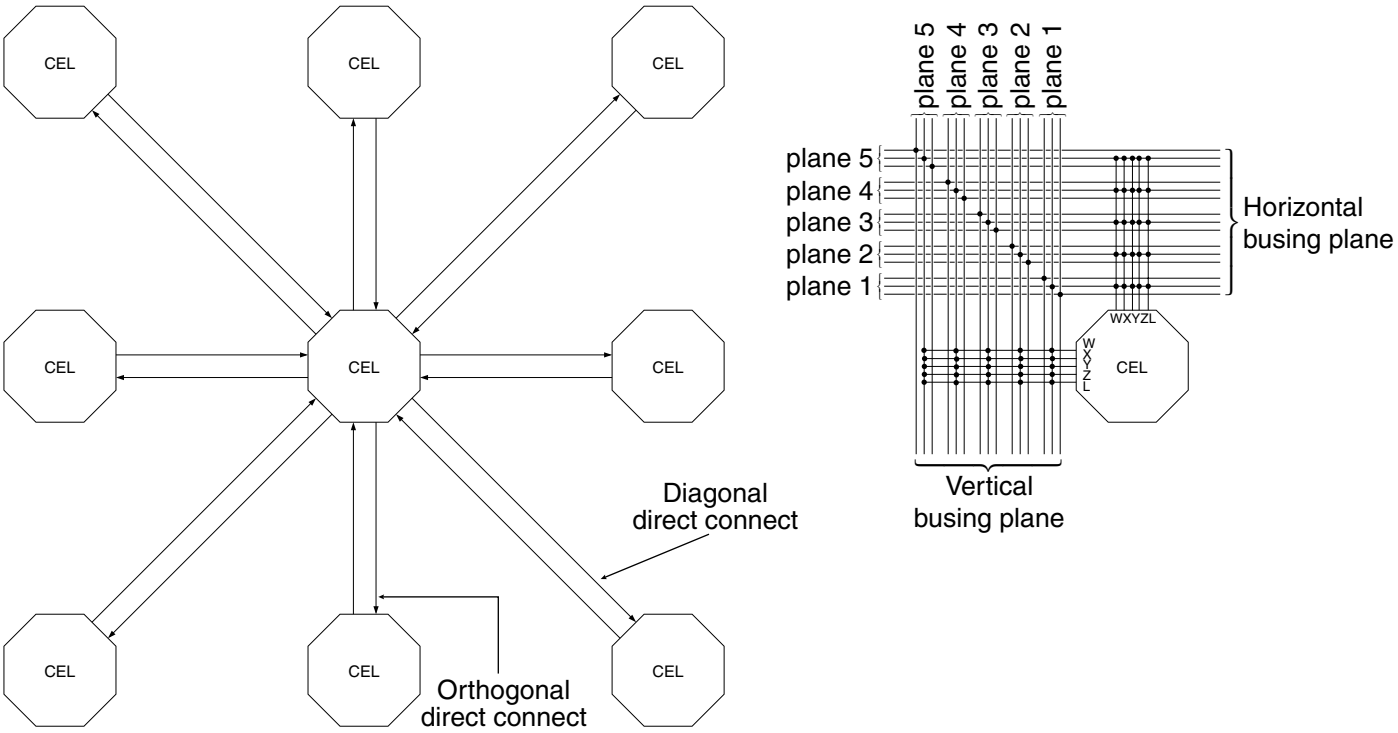
Figure 3. Busing Plane (One of Five)



Cell Connections

Figure 4(a) depicts direct connections between a cell and its eight nearest neighbors. Figure 4(b) shows the connections between a cell and five horizontal local buses (1 per busing plane) and five vertical local buses (1 per busing plane).

Figure 4. Cell Connections



(a) Cell-to-cell Connections

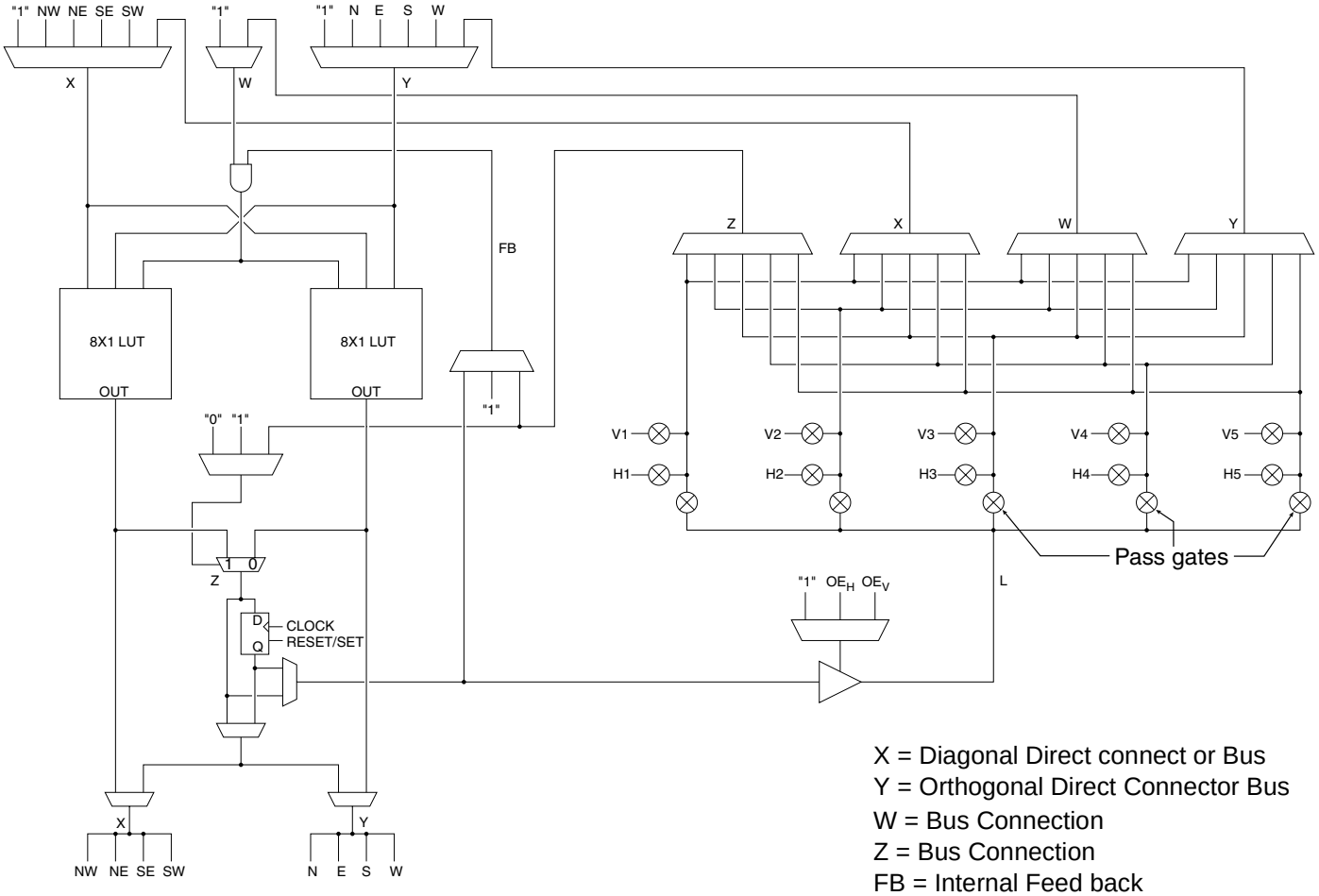
(b) Cell-to-bus Connections

The Cell

Figure 5 depicts the AT40KAL cell. Configuration bits for separate muxes and pass gates are independent. All permutations of programmable muxes and pass gates are legal. V_n (V_1 - V_5) is connected to the vertical local bus in plane n. H_n (H_1 - H_5) is connected to the horizontal local bus in plane n. A local/local turn in plane n is achieved by turning on the two pass gates connected to V_n and H_n. Pass gates are opened to let signals into the cell from a local bus or to drive a signal out onto a local bus. Signals coming into the logic cell on one local bus plane can be switched onto another plane by opening two of the pass gates. This allows bus signals to switch planes to achieve greater routability. Up to five simultaneous local/local turns are possible.

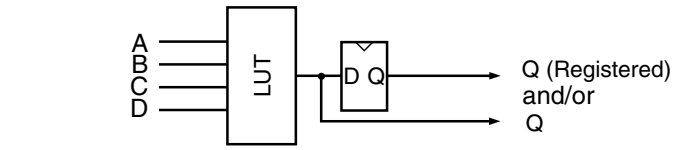
The AT40KAL FPGA core cell is a highly configurable logic block based around two 3-input LUTs (8 x 1 ROM), which can be combined to produce one 4-input LUT. This means that any core cell can implement two functions of 3 inputs or one function of 4 inputs. There is a Set/Reset D flip-flop in every cell, the output of which may be tri-stated and fed back internally within the core cell. There is also a 2-to-1 multiplexer in every cell, and an upstream AND gate in the “front end” of the cell. This AND gate is an important feature in the implementation of efficient array multipliers.

Figure 5. The Cell

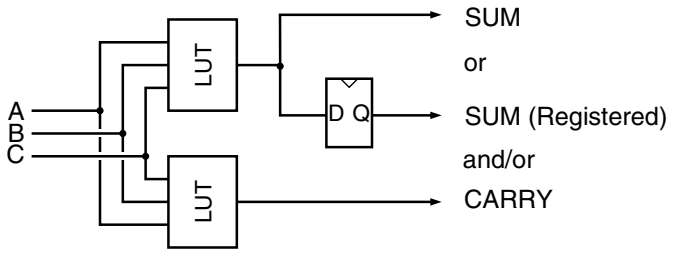


With this functionality in each core cell, the core cell can be configured in several “modes”. The core cell flexibility makes the AT40KAL architecture well suited to most digital design application areas (see Figure 6).

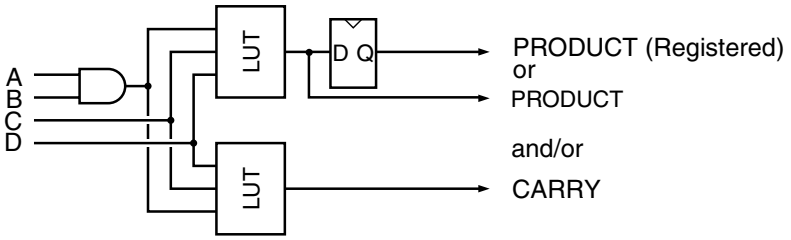
Figure 6. Some Single Cell Modes



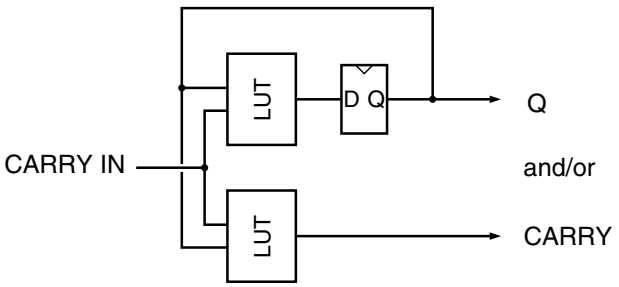
Synthesis Mode. This mode is particularly important for the use of VHDL design. VHDL Synthesis tools generally will produce as their output large amounts of random logic functions. Having a 4-input LUT structure gives efficient random logic optimization without the delays associated with larger LUT structures. The output of any cell may be registered, tri-stated and/or fed back into a core cell.



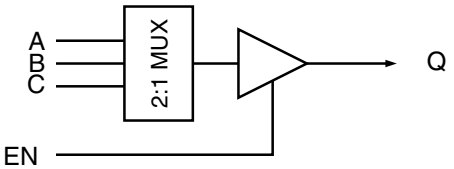
Arithmetic Mode is frequently used in many designs. As can be seen in the figure, the AT40K core cell can implement a 1-bit full adder (2-input adder with both Carry In and Carry Out) in one core cell. Note that the sum output in this diagram is registered. This output could then be tri-stated and/or fed back into the cell.



DSP/Multiplier Mode. This mode is used to efficiently implement array multipliers. An array multiplier is an array of bitwise multipliers, each implemented as a full adder with an upstream AND gate. Using this AND gate and the diagonal interconnects between cells, the array multiplier structure fits very well into the AT40K architecture.



Counter Mode. Counters are fundamental to almost all digital designs. They are the basis of state machines, timing chains and clock dividers. A counter is essentially an increment by one function (i.e., an adder), with the input being an output (or a decode of an output) from the previous stage. A 1-bit counter can be implemented in one core cell. Again, the output can be registered, tri-stated and/or fed back.

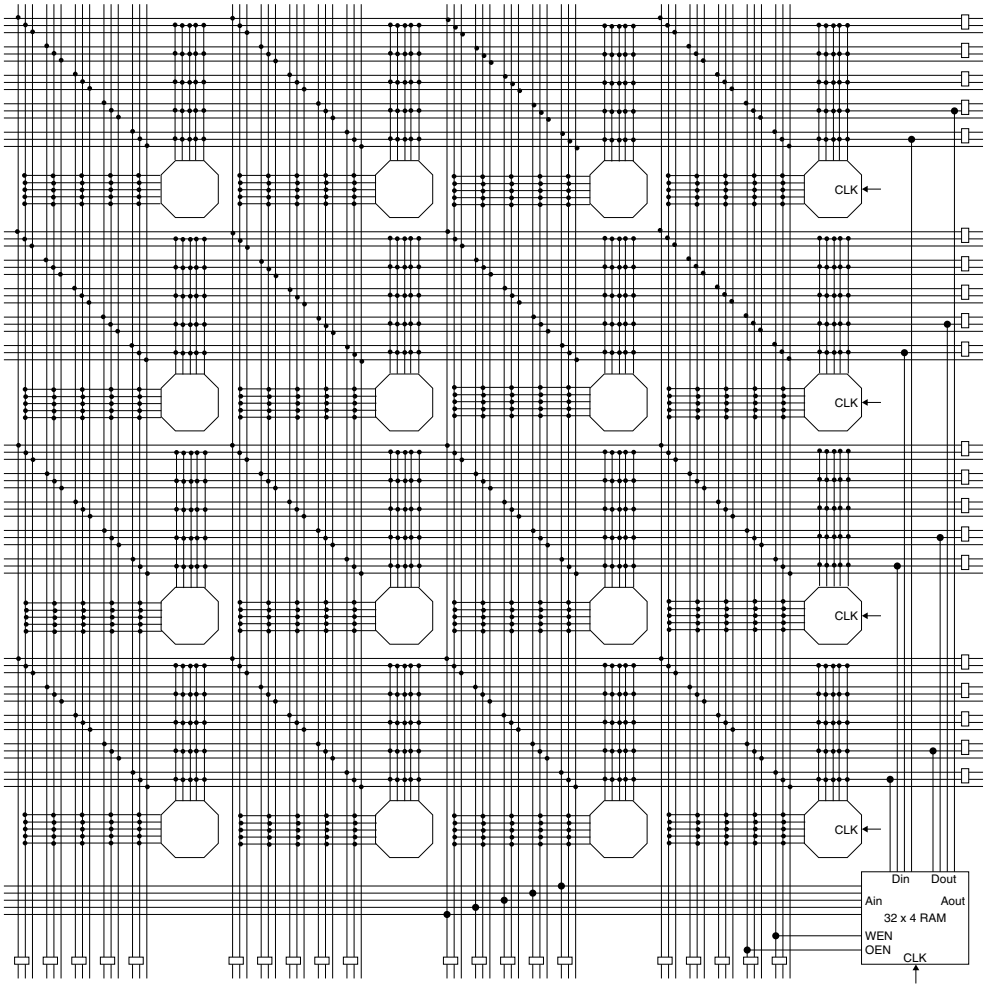


Tri-state/Mux Mode. This mode is used in many telecommunications applications, where data needs to be routed through more than one possible path. The output of the core cell is very often tri-statable for many inputs to many outputs data switching.

RAM

32 x 4 dual-ported RAM blocks are dispersed throughout the array as shown in Figure 7. A 4-bit Input Data Bus connects to four horizontal local buses distributed over four sector rows (plane 1). A 4-bit Output Data Bus connects to four horizontal local buses distributed over four sector rows (plane 2). A 5-bit Input Address Bus connects to five vertical express buses in same column. A 5-bit Output Address Bus connects to five vertical express buses in same column. Ain (input address) and Aout (output address) alternate positions in horizontally aligned RAM blocks. For the left-most RAM blocks, Aout is on the left and Ain is on the right. For the right-most RAM blocks, Ain is on the left and Aout is tied off, thus it can only be configured as a single port. For single-ported RAM, Ain is the READ/WRITE address port and Din is the (bi-directional) data port. Right-most RAM blocks can be used only for single-ported memories. WEN and OEN connect to the vertical express buses in the same column.

Figure 7. RAM Connections (One Ram Block)



Reading and writing of the 11 - 13 ns 32 x 4 dual-port FreeRAM are independent of each other. Reading the 32 x 4 dual-port RAM is completely asynchronous. Latches are transparent; when Load is logic 1, data flows through; when Load is logic 0, data is latched. These latches are used to synchronize Write Adress, Write Enable Not, and Din signals for a synchronous RAM. Each bit in the 32 x 4 dual-port RAM is also a transparent latch. The front-end latch and the memory latch together form an edge-triggered flip flop. When a nibble (bit = 7) is (Write) addressed and LOAD is logic 1 and $\overline{WE}$ is logic 0,

data flows through the bit. When a nibble is not (Write) addressed or LOAD is logic 0 or $\overline{WE}$ is logic 1, data is latched in the nibble. The two CLOCK muxes are controlled together; they both select CLOCK (for a synchronous RAM) or they both select “1” (for an asynchronous RAM). CLOCK is obtained from the clock for the sector-column immediately to the left and immediately above the RAM block. Writing any value to the RAM clear byte during configuration clears the RAM (see the “*AT40KAL/KEL Configuration Series”* application note at www.atmel.com).

Figure 8. RAM Logic

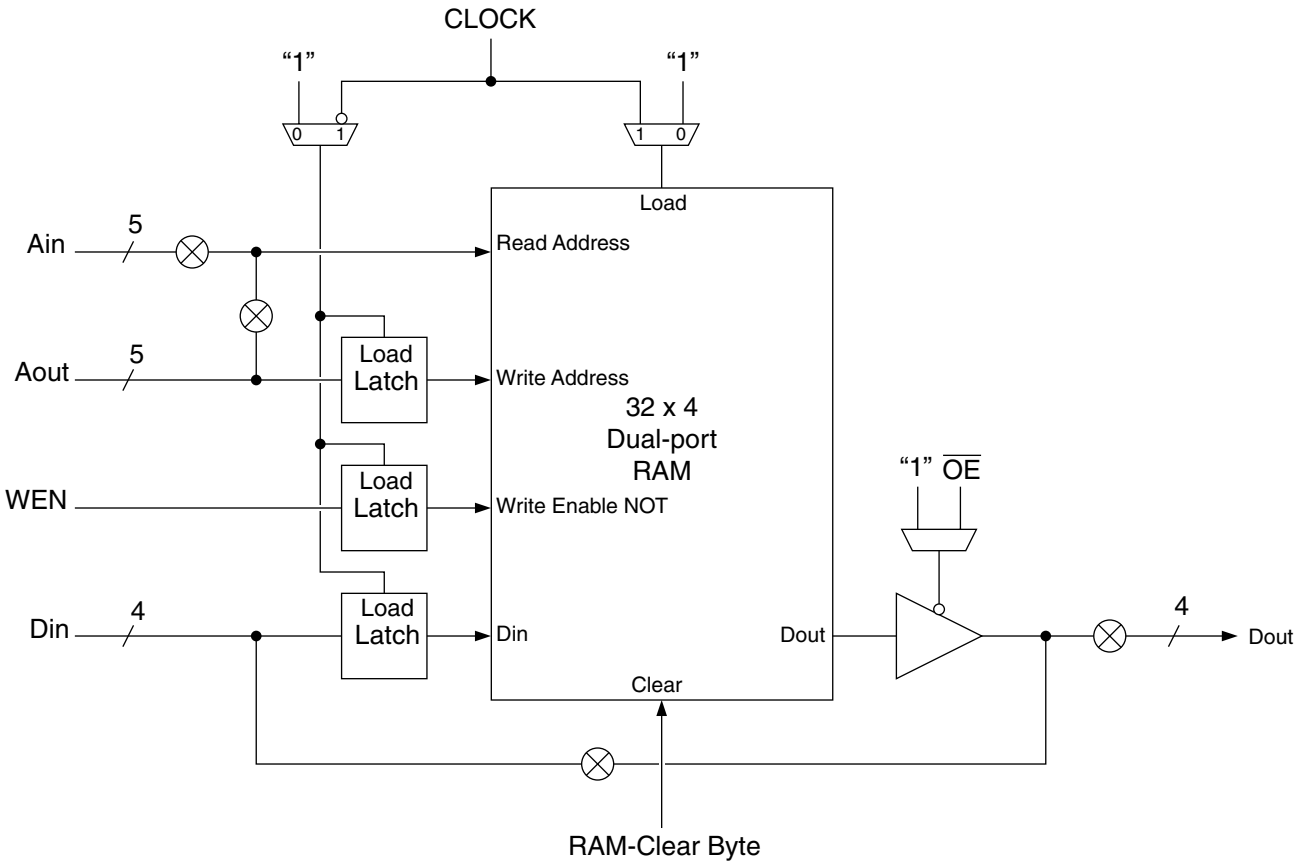
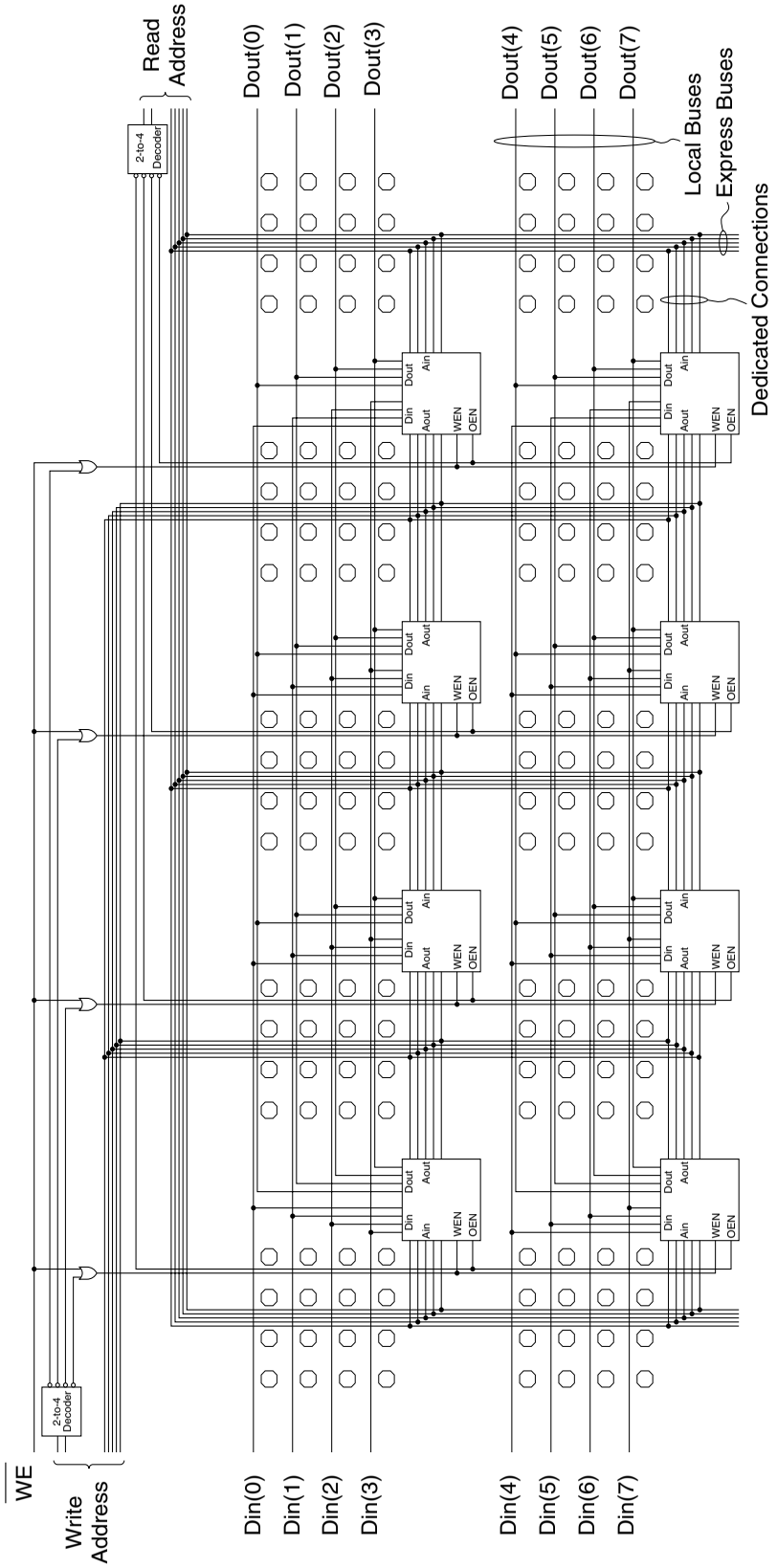


Figure 9 on page 13 shows an example of a RAM macro constructed using AT40KAL’s FreeRAM cells. The macro shown is a 128 x 8 dual-ported asynchronous RAM. Note the very small amount of external logic required to complete the address decoding for the macro. Most of the logic cells (core cells) in the sectors occupied by the RAM will be unused: they can be used for other logic in the design. This logic can be automatically generated using the macro generators.

Figure 9. RAM Example: 128 x 8 Dual-ported RAM (Asynchronous)



Clocking Scheme

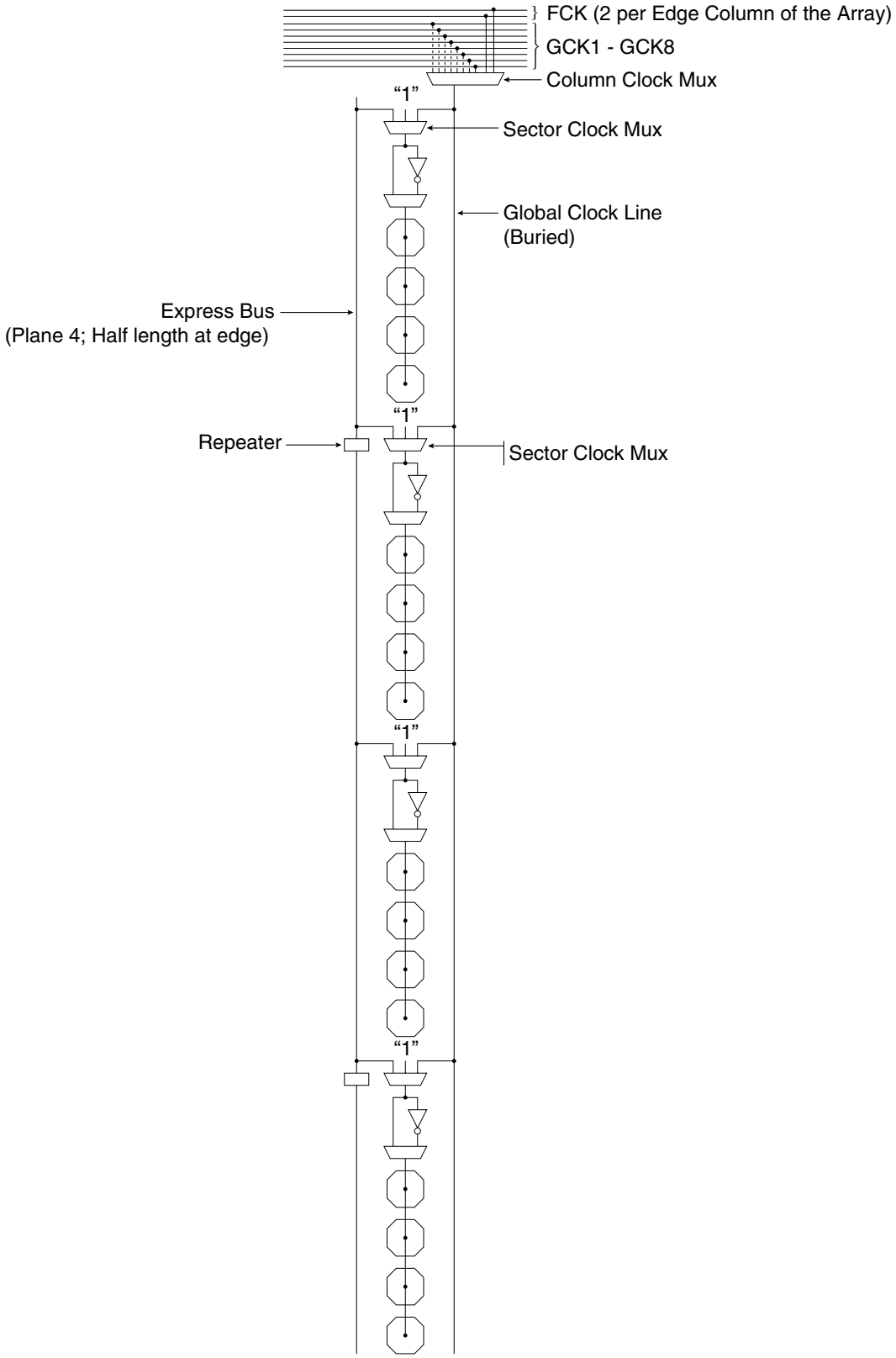
There are eight Global Clock buses (GCK1 - GCK8) on the AT40KAL FPGA. Each of the eight dedicated Global Clock buses is connected to one of the dual-use Global Clock pins. Any clocks used in the design should use global clocks where possible: this can be done by using Assign Pin Locks to lock the clocks to the Global Clock locations. In addition to the eight Global Clocks, there are four Fast Clocks (FCK1 - FCK4), two per edge column of the array for PCI specification. Even the derived clocks can be routed through the Global network. Access points are provided in the corners of the array to route the derived clocks into the global clock network. The IDS software tools handle derived clocks to global clock connections automatically if used.

Each column of an array has a “Column Clock mux” and a “Sector Clock mux”. The Column Clock mux is at the top of every column of an array and the Sector Clock mux is at every four cells. The Column Clock mux is selected from one of the eight Global Clock buses. The clock provided to each sector column of four cells is inverted, non-inverted or tied off to “0”, using the Sector Clock mux to minimize the power consumption in a sector that has no clocks. The clock can either come from the Column Clock or from the Plane 4 express bus (see Figure 10 on page 15). The extreme-left Column Clock mux has two additional inputs, FCK1 and FCK2, to provide fast clocking to left-side I/Os. The extreme-right Column Clock mux has two additional inputs as well, FCK3 and FCK4, to provide fast clocking to right-side I/Os.

The register in each cell is triggered on a rising clock edge by default. Before configuration on power-up, constant “0” is provided to each register’s clock pins. After configuration on power-up, the registers either set or reset, depending on the user’s choice.

The clocking scheme is designed to allow efficient use of multiple clocks with low clock skew, both within a column and across the core cell array.

Figure 10. Clocking (for One Column of Cells)



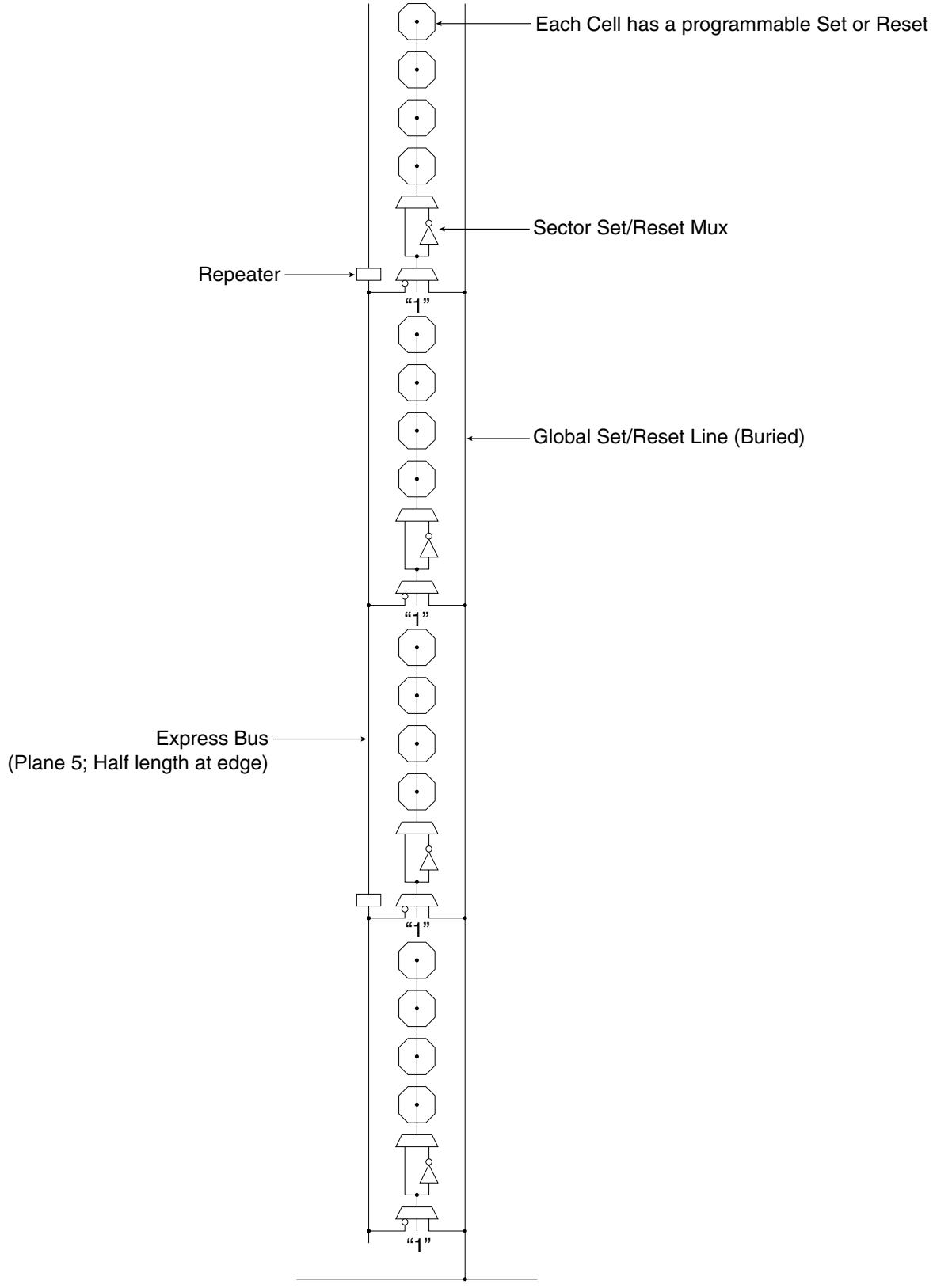
Set/Reset Scheme

The AT40KAL family reset scheme is essentially the same as the clock scheme except that there is only one Global Reset. A dedicated Global Set/Reset bus can be driven by any User I/O, except those used for clocking (Global Clocks or Fast Clocks). The automatic placement tool will choose the reset net with the most connections to use the global resources. You can change this by using an RSBUF component in your design to indicate the global reset. Additional resets will use the express bus network.

The Global Set/Reset is distributed to each column of the array. Like Sector Clock mux, there is Sector Set/Reset mux at every four cells. Each sector column of four cells is set/reset by a Plane 5 express bus or Global Set/Reset using the Sector Set/Reset mux (Figure 11 on page 17). The set/reset provided to each sector column of four cells is either inverted or non-inverted using the Sector Reset mux.

The function of the Set/Reset input of a register is determined by a configuration bit in each cell. The Set/Reset input of a register is active low (logic 0) by default. Setting or Resetting of a register is asynchronous. Before configuration on power-up, a logic 1 (a high) is provided by each register (i.e., all registers are set at power-up).

Figure 11. Set/Reset (for One Column of Cells)



I/O Structure

AT40KAL has registered I/Os and group enable every sector for tri-states on obuf's.

Pad

The I/O pad is the one that connects the I/O to the outside world. Note that not all I/Os have pads: the ones without pads are called Unbonded I/Os. The number of unbonded I/Os varies with the device size and package. These unbonded I/Os are used to perform a variety of bus turns at the edge of the array.

Pull-up/Pull-down

Each pad has a programmable pull-up and pull-down attached to it. This supplies a weak "1" or "0" level to the pad pin. When all other drivers are off, this control will dictate the signal level of the pad pin.

The input stage of each I/O cell has a number of parameters that can be programmed either as properties in schematic entry or in the I/O Pad Attributes editor in IDS.

CMOS

The threshold level is a CMOS-compatible level.

Schmitt

A Schmitt trigger circuit can be enabled on the inputs. The Schmitt trigger is a regenerative comparator circuit that adds 1V hysteresis to the input. This effectively improves the rise and fall times (leading and trailing edges) of the incoming signal and can be useful for filtering out noise.

Delays

The input buffer can be programmed to include four different intrinsic delays as specified in the AC timing characteristics. This feature is useful for meeting data hold requirements for the input signal.

Drive

The output drive capabilities of each I/O are programmable. They can be set to FAST, MEDIUM or SLOW (using IDS tool). The FAST setting has the highest drive capability (16 mA at 5V) buffer and the fastest slew rate. MEDIUM produces a medium drive (12 mA at 5V) buffer, while SLOW yields a standard (4 mA at 5V) buffer.

Tri-State

The output of each I/O can be made tri-state (0, 1 or Z), open source (1 or Z) or open drain (0 or Z) by programming an I/O's Source Selection mux. Of course, the output can be normal (0 or 1), as well.

Source Selection Mux

The Source Selection mux selects the source for the output signal of an I/O. See Figure 12 on page 21.

Primary, Secondary and Corner I/Os

The AT40KAL has three kinds of I/Os: Primary I/O, Secondary I/O and a Corner I/O. Every edge cell except corner cells on the AT40KAL has access to one Primary I/O and two Secondary I/Os.

Primary I/O

Every logic cell at the edge of the FPGA array has a direct orthogonal connection to and from a Primary I/O cell. The Primary I/O interfaces directly to its adjacent core cell. It also connects into the repeaters on the row immediately above and below the adjacent core cell. In addition, each Primary I/O also connects into the busing network of the three nearest edge cells. This is an extremely powerful feature, as it provides logic cells toward the center of the array with fast access to I/Os via local and express buses. It can be seen from the diagram that a given Primary I/O can be accessed from any logic cell on three separate rows or columns of the FPGA. See Figures 12a and 13a.

Secondary I/O

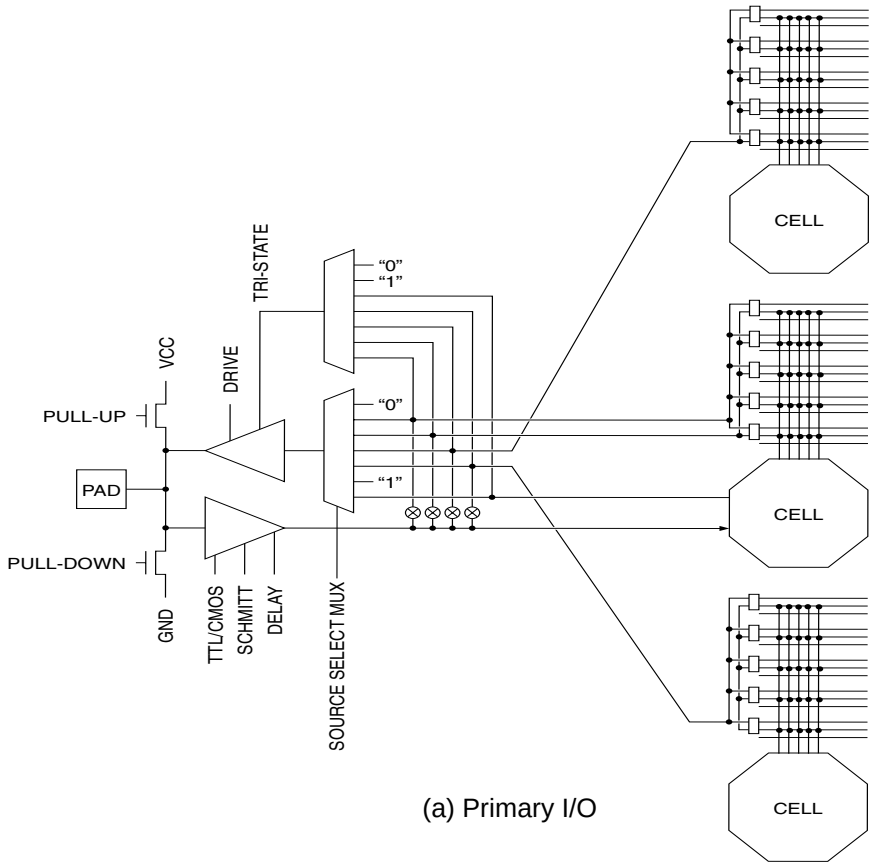
Every logic cell at the edge of the FPGA array has two direct diagonal connections to a Secondary I/O cell. The Secondary I/O is located between core cell locations. This I/O

connects on the diagonal inputs to the cell above and the cell below. It also connects to the repeater of the cell above and below. In addition, each Secondary I/O also connects into the busing network of the two nearest edge cells. This is an extremely powerful feature, as it provides logic cells toward the center of the array with fast access to I/Os via local and express buses. It can be seen from the diagram that a given Secondary I/O can be accessed from any logic cell on two rows or columns of the FPGA. See Figure 12a and Figure 13b.

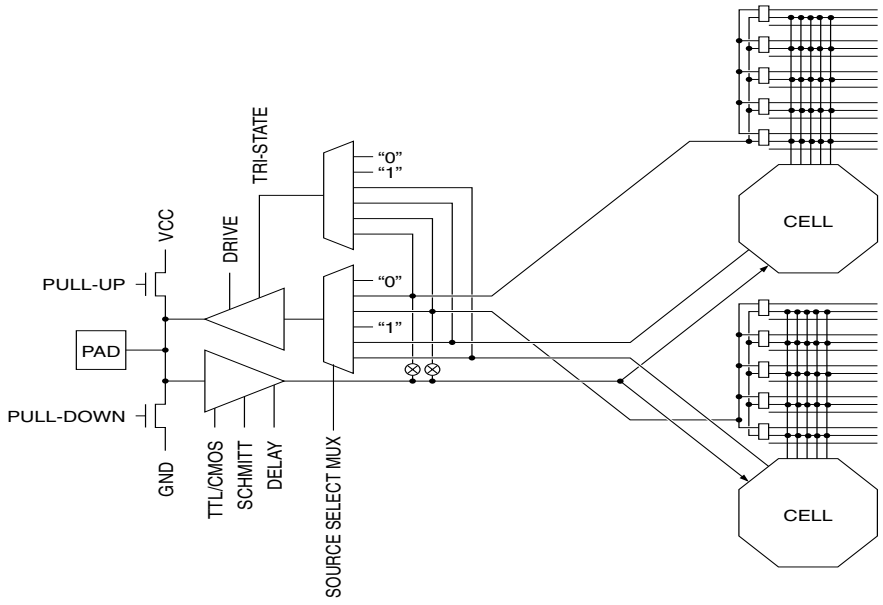
Corner I/O

Logic cells at the corner of the FPGA array have direct-connect access to five separate I/Os: 2 Primary, 2 Secondary and 1 Corner I/O. Corner I/Os are like an extra Secondary I/O at each corner of the array. With the inclusion of Corner I/Os, an AT40KAL FPGA with n x n core cells always has 8n I/Os. As the diagram shows, Corner I/Os can be accessed both from the corner logic cell and the horizontal and vertical busing networks running along the edges of the array. This means that many different edge logic cells can access the Corner I/Os. See Figure 14.

Figure 12. South I/O (Mirrored for North I/O)

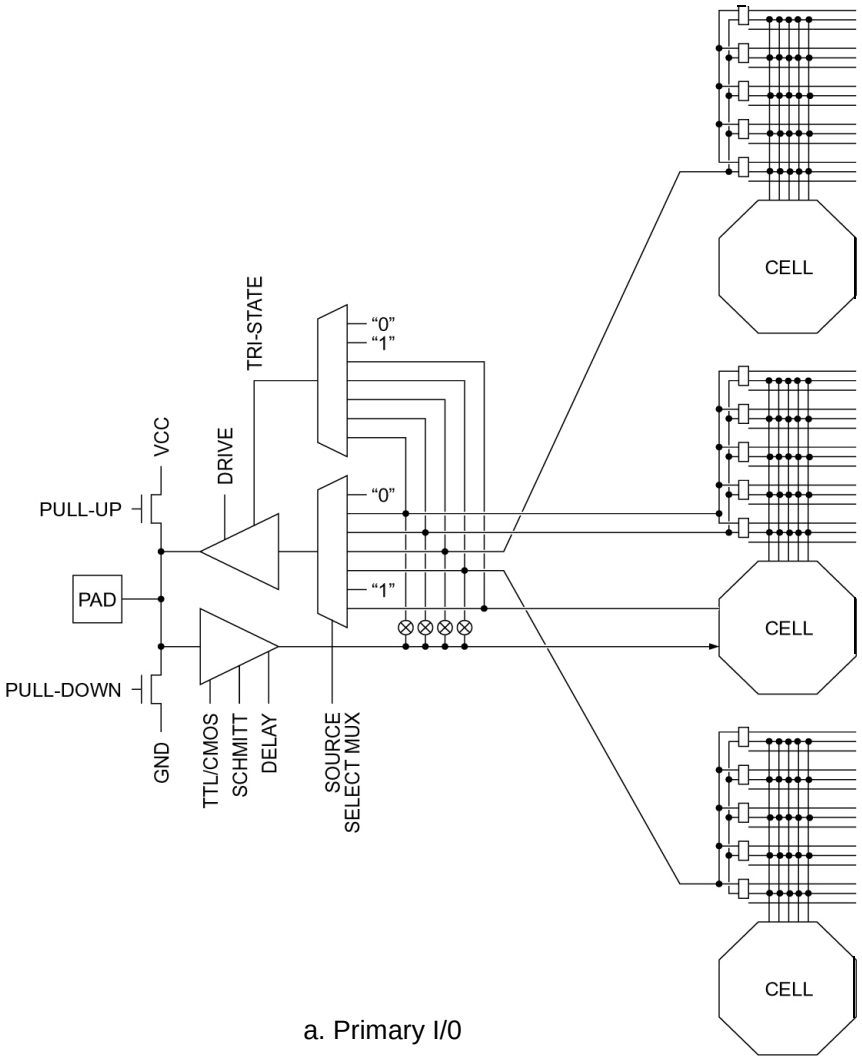


(a) Primary I/O

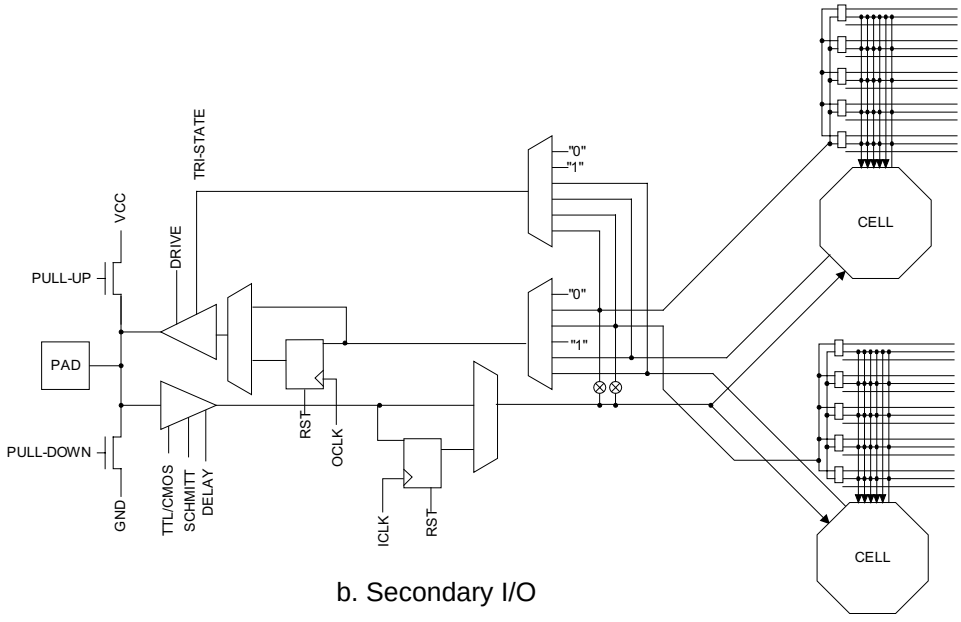


(b) Secondary I/O

Figure 13. West I/O (Mirrored for East I/O)

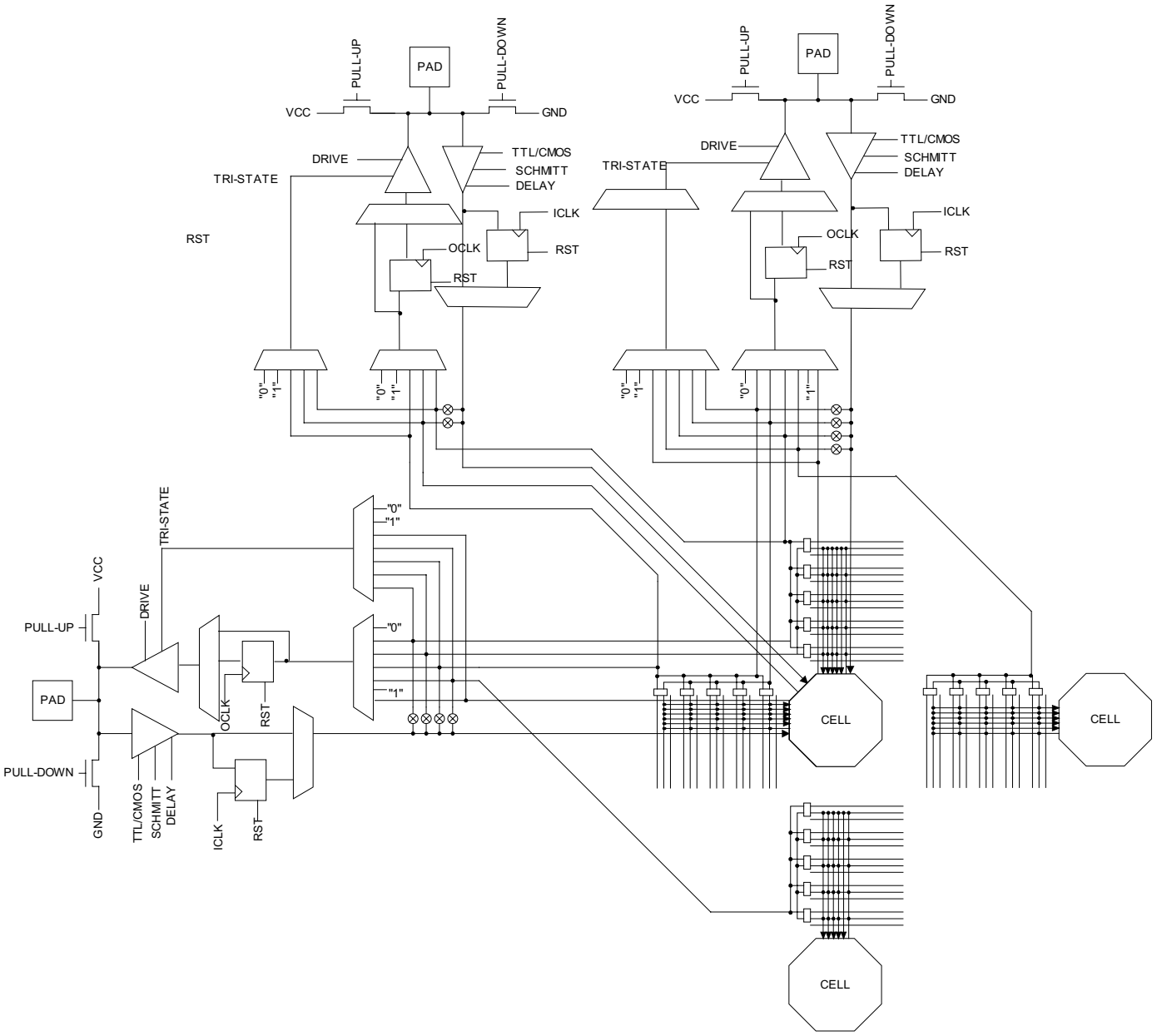


a. Primary I/0



b. Secondary I/O

Figure 14. Northwest Corner I/O (Similar NE/SE/SW Corners)



Electrical Characteristics

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Junction Temperature	+150°C
Voltage on Any Pin with Respect to Ground (1)	-0.5V to V_{CC} +0.5V
Supply Voltage (V_{CC})	5V ± 10%
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	4000V

*Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

1. For DC Input Voltage (V_I) Minimum voltage of -0.5V DC, which may undershoot to -2.0V for pulses of less than 20 ns.

DC and AC Operating Range

Operating Temperature		-55°C to +125°C
V_{CC} Power Supply		3.3V ± 0.3V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage	CMOS	70% V_{CC}			V
		TTL	2.0			V
V_{IL}	Low-level Input Voltage	CMOS	-0.3		30% V_{CC}	V
		TTL	-0.3		0.8	V
V_{OH}	High-level Output Voltage	I_{OH} = 4 mA V_{CC} = V_{CC} min	2.4			V
		I_{OH} = 12 mA V_{CC} = 3.0V	2.4			V
		I_{OH} = 16 mA V_{CC} = 3.0V	2.4			V
V_{OL}	Low-level Output Voltage	I_{OL} = -4 mA V_{CC} = 3.0V			0.4	V
		I_{OL} = -12 mA V_{CC} = 3.0V			0.4	V
		I_{OL} = -16 mA V_{CC} = 3.0V			0.4	V
I_{IH}	High-level Input Current	V_{IN} = V_{CC} max	-5		5	µA
		With pull-down, V_{IN} = V_{CC}	20	75	300.0	µA
I_{IL}	Low-level Input Current	V_{IN} = V_{SS}	-5		5	µA
		With pull-up, V_{IN} = V_{SS}	-300.0	-50	-20	µA
I_{OZH}	High-level Tri-state Output Leakage Current	Without pull-down, V_{IN} = V_{CC} max	-5		5	µA
		With pull-down, V_{IN} = V_{CC} max	20		300.0	µA
I_{OZL}	Low-level Tri-state Output Leakage Current	Without pull-up, V_{IN} = V_{SS}	-5		5	mA
		With pull-up, V_{IN} = V_{SS} for CON	-500	-150.0	-110	µA
I_{CC}	Standby Current Consumption	Standby, unprogrammed		1	5	mA
C_{IN}	Input Capacitance	All pins			10.0	pF

Note: 1. Parameter based on characterization and simulation; it is not tested in production.

Power-On Power Supply Requirements

Atmel FPGAs require a minimum rated power supply current capacity to ensure proper initialization, and the power supply ramp-up time does not affect the current required. A fast ramp-up time requires more current than a slow ramp-up time.

Table 3. Power-on Supply Requirements

Description	Maximum Current[1][2]
Maximum Current Supply	100 mA

Note: 1. Devices are guaranteed to initialize properly at 50% of the minimum current listed above. A larger capacity power supply may result in a larger initiallization current.

2. Ramp-up time is measured from 0V DC to 3.6V DC. Peak current required lasts less than 2 ms, and occurs near the internal power on reset threshold voltage.

AC Timing Characteristics

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{cc} = 3.0V, temperature = 125°C.
Minimum times based on best case: V_{cc} = 3.60V, temperature = -55°C.
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	AT40KAL	Units	Notes
Core					
2-input gate	t_{PD} (max)	x/y -> x/y	1.9	ns	1 unit load
3-input gate	t_{PD} (max)	x/y/z -> x/y	2.3	ns	1 unit load
3-input gate	t_{PD} (max)	x/y/w -> x/y	2.5	ns	1 unit load
4-input gate	t_{PD} (max)	x/y/w/z -> x/y	2.5	ns	1 unit load
Fast carry	t_{PD} (max)	y -> y	1.8	ns	1 unit load
Fast carry	t_{PD} (max)	x -> y	1.7	ns	1 unit load
Fast crry	t_{PD} (max)	y -> x	1.8	ns	1 unit load
Fast carry	t_{PD} (max)	x -> x	1.9	ns	1 unit load
Fast carry	t_{PD} (max)	w -> y	2.4	ns	1 unit load
Fast carry	t_{PD} (max)	w -> x	2.5	ns	1 unit load
Fast carry	t_{PD} (max)	z -> y	2.3	ns	1 unit load
Fast carry	t_{PD} (max)	z -> x	2.3	ns	1 unit load
DFF	t_{PD} (max)	clk -> x/y	2.1	ns	1 unit load
DFF	t_{PD} (max)	R -> x/y	2.8	ns	1 unit load
DFF	t_{PD} (max)	S -> x/y	2.9	ns	1 unit load
DFF	t_{PD} (max)	q -> w	2.2	ns	
Incremental -> L	t_{PD} (max)	x/y -> L	1.7	ns	1 unit load
Local output enable	t_{PZX} (max)	oe -> L	1.5	ns	1 unit load
Local output enable	t_{PXZ} (max)	oe -> L	0.8	ns	

AC Timing Characteristics

All input I/O characteristics measured from V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD}.
All output I/O characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Cell Function	Parameter	Path	AT40KAL	Units	Notes
Repeaters					
Repeater	t_{PD} (max)	L -> E	1.2	ns	1 unit load
Repeater	t_{PD} (max)	E -> E	1.2	ns	1 unit load
Repeater	t_{PD} (max)	L -> L	1.2	ns	1 unit load
Repeater	t_{PD} (max)	E -> L	1.2	ns	1 unit load
Repeater	t_{PD} (max)	E -> IO	0.5	ns	1 unit load
Repeater	t_{PD} (max)	L -> IO	0.5	ns	1 unit load

Cell Function	Parameter	Path	AT40KAL	Units	Notes
I/O					
Input	t_{PD} (max)	pad -> x/y	2.7	ns	no extra delay
Input	t_{PD} (max)	pad -> x/y	4.9	ns	1 extra delay
Input	t_{PD} (max)	pad -> x/y	8.1	ns	2 extra delays
Input	t_{PD} (max)	pad -> x/y	11.3	ns	3 extra delays
Output, slow	t_{PD} (max)	x/y/E/L -> pad	11.2	ns	50 pf load
Output, medium	t_{PD} (max)	x/y/E/L -> pad	8.4	ns	50 pf load
Output, fast	t_{PD} (max)	x/y/E/L -> pad	6.9	ns	50 pf load
Output, slow	t_{PZX} (max)	oe -> pad	12.2	ns	50 pf load
Output, slow	t_{PXZ} (max)	oe -> pad	1.9	ns	50 pf load
Output, medium	t_{PZX} (max)	oe -> pad	7.8	ns	50 pf load
Output, medium	t_{PXZ} (max)	oe -> pad	3.3	ns	50 pf load
Output, fast	t_{PZX} (max)	oe -> pad	6.1	ns	50 pf load
Output, fast	t_{PXZ} (max)	oe -> pad	3.3	ns	50 pf load

AC Timing Characteristics

Clocks and Reset Input buffers are measured from a V_{IH} of 1.5V at the input pad to the internal V_{IH} of 50% of V_{CC}. Maximum times for clock input buffers and internal drivers are measured for rising edge delays only.

Cell Function	Parameter	Path	Device		Units	Notes
Global Clocks and Set/Reset						
GCK Input buffer	t_{PD} (max)	pad -> clock	AT40KAL	2.5	ns	rising edge clock
FCK Input buffer	t_{PD} (max)	pad -> clock	AT40KAL	1.9	ns	rising edge clock
Clock column driver	t_{PD} (max)	clock -> colclk	AT40KALAT 40KAL	1.1	ns	rising edge clock
Clock sector driver	t_{PD} (max)	colclk -> secclk	AT40KAL	0.7	ns	rising edge clock
GSRN Input buffer	t_{PD} (max)	colclk -> secclk	AT40KAL	7.2	ns	
Global clock to output	t_{PD} (max)	clock pad -> out	AT40KAL	13.4	ns	rising edge clock fully loaded clock tree rising edge DFF 20 mA output buffer 50 pf pin load
Fast clock to output	t_{PD} (max)	clock pad -> out	AT40KAL	12.4	ns	rising edge clock fully loaded clock tree rising edge DFF 20 mA output buffer 50 pf pin load

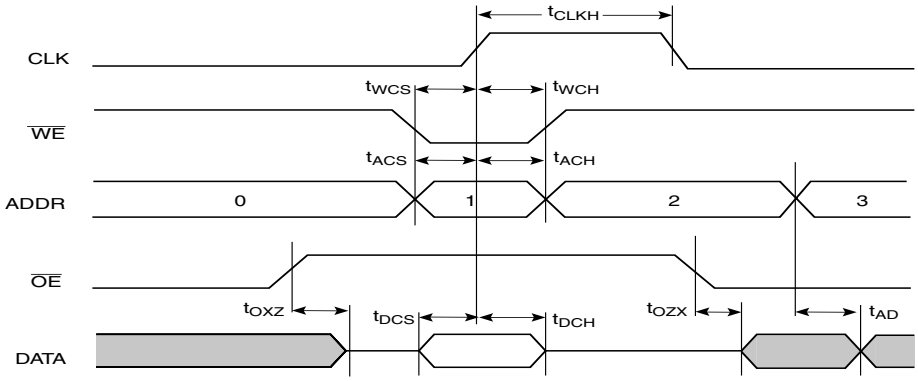
Notes:
1. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. Buffer delay is to a pad voltage of 1.5V with one output switching.
3. Parameter based on characterization and simulation; not tested in production.
4. Exact power calculation is available in Atmel FPGA Designer software.

AC Timing Characteristics

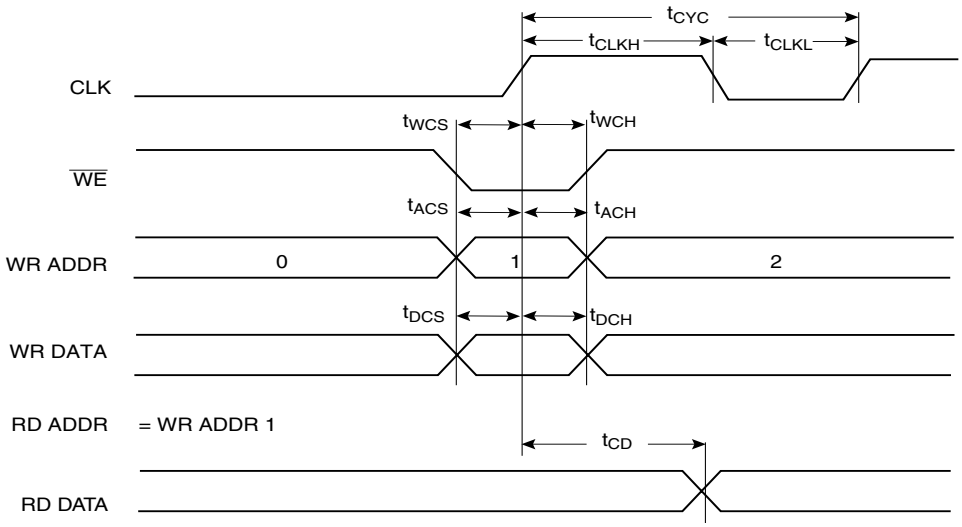
Cell Function	Parameter	Path	AT40KAL	Units	Notes
Async RAM					
Write	t_{WECYC} (min)	cycle time	14	ns	
Write	t_{WEL} (min)	we	5.5	ns	pulse width low
Write	t_{WEH} (min)	we	5.5	ns	pulse width high
Write	t_{setup} (min)	wr addr setup -> we	5.8	ns	
Write	t_{hold} (min)	wr addr hold -> we	0.0	ns	
Write	t_{setup} (min)	din setup -> we	5.0	ns	
Write	t_{hold} (min)	din hold -> we	0.0	ns	
Write	t_{hold} (min)	oe hold -> we	0.0	ns	
Write/Read	t_{PD} (max)	din -> dout	7.0	ns	rd addr = wr addr
Read	t_{PD} (max)	rd addr -> dout	4.8	ns	
Read	t_{PZX} (max)	oe -> dout	3.3	ns	
Read	t_{PXZ} (max)	oe -> dout	3.3	ns	
Sync RAM					
Write	t_{CYC} (min)	cycle time	14	ns	
Write	t_{CLKL} (min)	clk	5.5	ns	pulse width low
Write	t_{CLKH} (min)	clk	5.5	ns	pulse width high
Write	t_{setup} (min)	we setup -> clk	3.5	ns	
Write	t_{hold} (min)	we hold -> clk	0.0	ns	
Write	t_{setup} (min)	wr addr setup -> clk	5.5	ns	
Write	t_{hold} (min)	wr addr hold -> clk	0.0	ns	
Write	t_{setup} (min)	wr data setup -> clk	4.3	ns	
Write	t_{hold} (min)	wr data hold -> clk	0.0	ns	
Write/Read	t_{PD} (max)	din -> dout	7.0	ns	rd addr = wr addr
Write/Read	t_{PD} (max)	clk -> dout	4.9	ns	rd addr = wr addr
Read	t_{PD} (max)	rd addr -> dout	4.8	ns	
Read	t_{PZX} (max)	oe -> dout	3.3	ns	
Read	t_{PXZ} (max)	oe -> dout	3.3	ns	

FreeRAM Asynchronous Timing Characteristics

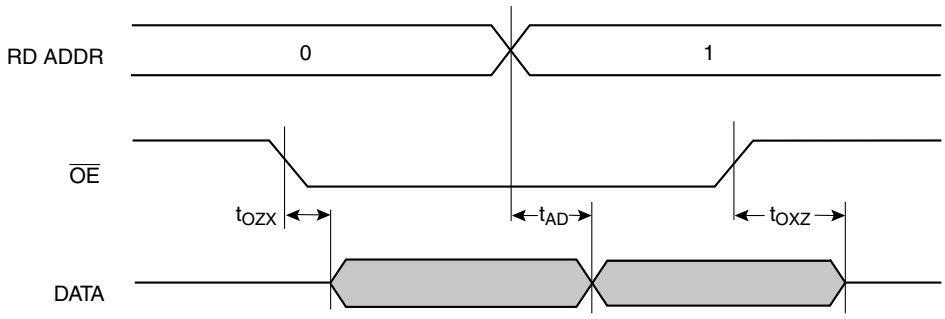
Single Port Write/Read



Dual Port Write with Read

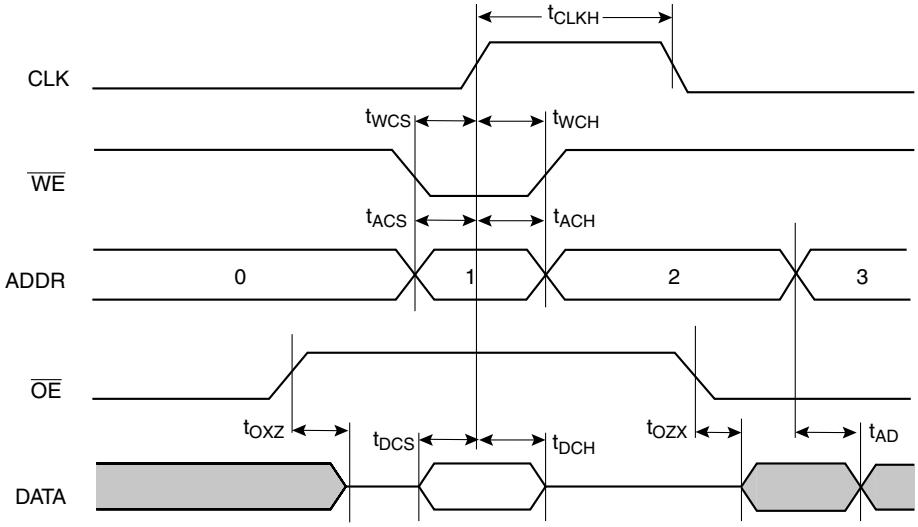


Dual Port Read

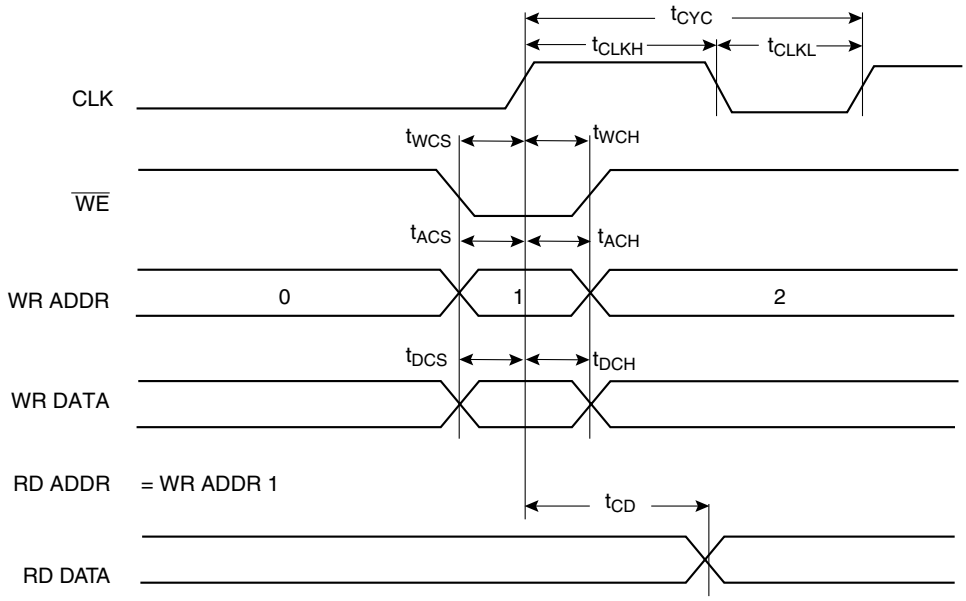


FreeRAM Synchronous Timing Characteristics

Single Port Write/Read



Dual Port Write with Read



Dual Port Read

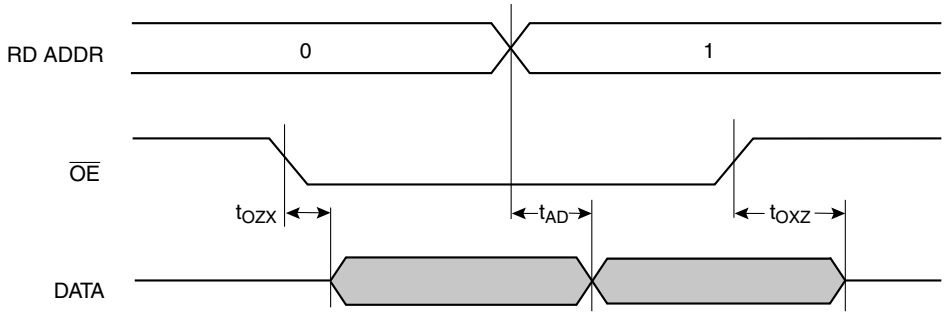


Table 4. Pad/Pin Assignment

384 I/O	MQFPF160
GND	1
I/O1, GCK1 (A16)	2
I/O2 (A17)	3
I/O3	4
I/O4	5
I/O5 (A18)	6
I/O6 (A19)	7
GND	
I/O7	
I/O8	
I/O9	
I/O10	
I/O11	
I/O12	
VCC	
GND	
I/O13	
I/O14	
I/O15	8
I/O16	9
I/O17	
I/O18	
GND	
I/O19	
I/O20	
I/O21	
I/O22	
I/O23	
I/O24	
GND	10
I/O25, FCK1	11
I/O26	12
I/O27 (A20)	13
I/O28 (A21)	14
VCC	
I/O29	
I/O30	
GND	

384 I/O	MQFPF160
I/O31	
I/O32	
I/O33	
I/O34	
I/O35	
I/O36	
GND	
VCC	
I/O37	
I/O38	
I/O39	
I/O40	
I/O41	
I/O42	
GND	
I/O43	15
I/O44	16
I/O45	
I/O46	
I/O47 (A22)	17
I/O48 (A23)	18
GND	19
VCC	20
I/O49	21
I/O50	22
I/O51	
I/O52	
I/O53	23
I/O54	24
GND	
I/O55	
I/O56	
I/O57	
I/O58	
I/O59	
I/O60	
VCC	
GND	
I/O61	
I/O62	
I/O63	
I/O64	
I/O65	

384 I/O	MQFPF160
I/O66	
GND	
I/O67	
I/O68	
VCC	
I/O69	25
I/O70	26
I/O71	27
I/O72, FCK2	28
GND	29
I/O73	
I/O74	
I/O75	
I/O76	
I/O77	
I/O78	
GND	
I/O79	
I/O80	
I/O81	
I/O82	
I/O83	30
I/O84	31
GND	
VCC	
I/O85	
I/O86	
I/O87	
I/O88	
I/O89	32
I/O90	33
GND	
I/O91	
I/O92	
I/O93	34
I/O94	35
I/O95 ($\overline{\text{OTS}}$)[1]	36
I/O96, GCK2	37
M1	38
GND	39
M0	40
VCC	41
M2	42

384 I/O	MQFPF160
I/O97, GCK3	43
I/O98 (HDC)	44
I/O99	45
I/O100	46
I/O101	47
I/O102 (LDC)	48
GND	
I/O103	
I/O104	
I/O105	
I/O106	
I/O107	
I/O108	
VCC	
GND	
I/O109	49
I/O110	50
I/O111	
I/O112	
I/O113	
I/O114	
GND	
I/O115	
I/O116	
I/O117	
I/O118	
I/O119	
I/O120	
GND	51
I/O121	52
I/O122	53
I/O123	54
I/O124	55
VCC	
I/O125	
I/O126	
GND	
I/O127	
I/O128	
I/O129	
I/O130	
I/O131	
I/O132	

384 I/O	MQFPF160
GND	
VCC	
I/O133	
I/O134	
I/O135	
I/O136	
I/O137	56
I/O138	57
GND	
I/O139	
I/O140	
I/O141	
I/O142	
I/O143 (D15)	58
I/O144 (INIT)	59
VCC	60
GND	61
I/O145 (D14)	62
I/O146 (D13)	63
I/O147	
I/O148	
I/O149	
I/O150	
GND	
I/O151	64
I/O152	65
I/O153	
I/O154	
I/O155	
I/O156	
VCC	
GND	
I/O157	
I/O158	
I/O159	
I/O160	
I/O161	
I/O162	
GND	
I/O163	
I/O164	
VCC	

384 I/O	MQFPF160
I/O165 (D12)	66
I/O166 (D11)	67
I/O167	68
I/O168	69
GND	70
I/O169	
I/O170	
I/O171	
I/O172	
I/O173	
I/O174	
GND	
I/O175	
I/O176	
I/O177	
I/O178	
I/O179	71
I/O180	72
GND	
VCC	
I/O181	
I/O182	
I/O183 (D10)	73
I/O184 (D9)	74
I/O185	
I/O186	
GND	
I/O187	
I/O188	
I/O189	75
I/O190	76
I/O191 (D8)	77
I/O192, GCK4	78
GND	79
$\overline{\text{CON}}$	80
VCC	81
$\overline{\text{RESET}}$	82
I/O193 (D7)	83
I/O194, GCK5	84
I/O195	85

384 I/O	MQFPF160
I/O196	86
I/O197	
I/O198	
GND	
I/O199	
I/O200	
I/O201	
I/O202	
I/O203	
I/O204	
VCC	
GND	
I/O205 (D6)	87
I/O206	88
I/O207	89
I/O208	90
I/O209	
I/O210	
GND	
I/O211	
I/O212	
I/O213	
I/O214	
I/O215	
I/O216	
GND	91
I/O217	
I/O218	
I/O219, FCK3	92
I/O220	93
VCC	
I/O221 (D5)	94
I/O222 (CS0)	95
GND	
I/O223	
I/O224	
I/O225	
I/O226	
I/O227	
I/O228	
GND	
VCC	

384 I/O	MQFPF160
I/O229	
I/O230	
I/O231	
I/O232	
I/O233	
I/O234	
GND	
I/O235	96
I/O236	97
I/O237	
I/O238	
I/O239(D4)	98
I/O240	99
VCC	100
GND	101
I/O241 (D3)	102
I/O242 ($\overline{\text{CHECK}}$)	103
I/O243	
I/O244	
I/O245	104
I/O246	105
GND	
I/O247	
I/O248	
I/O249	
I/O250	
I/O251	
I/O252	
VCC	
GND	
I/O253	
I/O254	
I/O255	
I/O256	
I/O257	
I/O258	
GND	
I/O259 (D2)	106
I/O260	107
VCC	
I/O261	108
I/O262,FCK4	109
I/O263	

384 I/O	MQFPF160
I/O264	
GND	110
I/O265	
I/O266	
I/O267	
I/O268	
I/O269	
I/O270	
GND	
I/O271	
I/O272	
I/O273	111
I/O274	112
I/O275	
I/O276	
GND	
VCC	
I/O277 (D1)	113
I/O278	114
I/O279	
I/O280	
I/O281	
I/O282	
GND	
I/O283	
I/O284	
I/O285	115
I/O286	116
I/O287 (D0)	117
I/O288, $\overline{\text{GCK6}}$ ($\overline{\text{CSOUT}}$)	118
CCLK	119
VCC	120
TSTCLK	121
GND	122
I/O289 (A0)	123
I/O290, GCK7 (A1)	124
I/O291	125
I/O292	126
I/O293	
I/O294	
GND	

384 I/O	MQFPF160
I/O295	
I/O296	
I/O297 ($\overline{CS1}$,A2)	127
I/O298 (A3)	128
I/O299	
I/O300	
VCC	
GND	
I/O301[1]	121[1] NC
I/O302	
I/O303	129
I/O304	130
I/O305	
I/O306	
GND	
I/O307	
I/O308	
I/O309	
I/O310	
I/O311	
I/O312	
GND	131
I/O313	132
I/O314	133
I/O315	
I/O316	
VCC	
I/O317	
I/O318	
GND	
I/O319	
I/O320	
I/O321	
I/O322	
I/O323	
I/O324	
GND	
VCC	
I/O325 (A4)	134
I/O326 (A5)	135
I/O327	
I/O328	136

384 I/O	MQFPF160
I/O329	137
I/O330	138
GND	
I/O331	
I/O332	
I/O333	
I/O334	
I/O335 (A6)	139
I/O336 (A7)	140
GND	141
VCC	142
I/O337 (A8)	143
I/O338 (A9)	144
I/O339	
I/O340	
I/O341	
I/O342	
GND	
I/O343	145
I/O344	146
I/O345	
I/O346	
I/O347 (A10)	147
I/O348 (A11)	148
VCC	
GND	
I/O349	
I/O350	
I/O351	
I/O352	
I/O353	
I/O354	
GND	
I/O355	
I/O356	
VCC	
I/O357	
I/O358	
I/O359	149
I/O360	150
GND	151

384 I/O	MQFPF160
I/O361	
I/O362	
I/O363	
I/O364	
I/O365	
I/O366	
GND	
I/O367	
I/O368	
I/O369	152
I/O370	153
I/O371 (A12)	154
I/O372 (A13)	155
GND	
VCC	
I/O373	
I/O374	
I/O375	
I/O376	
I/O377	
I/O378	
GND	
I/O379	
I/O380	
I/O381	156
I/O382	157
I/O383 (A14)	158
I/O384, GCK8 (A15)	159
VCC	160

Note: 1. Shared with TSTCLK

Part/Package Availability and User I/O Counts (Including Dual-function Pins)

Package	AT40KAL
MQFPF 160	130
MQFPF 256[1]	193
MQFPF 352[1]	289

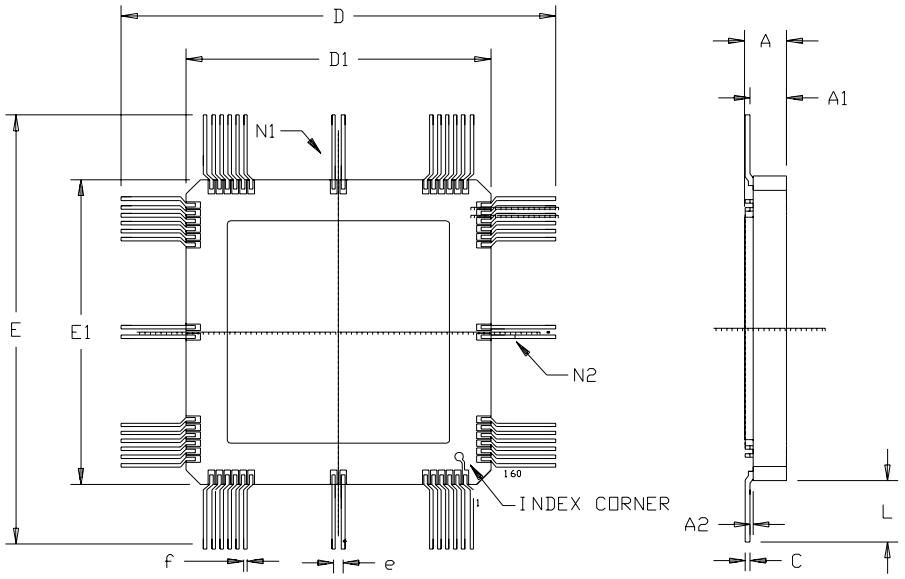
Note: 1. Contact Atmel for availabilty.

Ordering Information

Part Number	Temperature Range	Quality Flow
AT40KAL040KW1M-E	25°C	Engineering Samples
AT40KAL040KW1M	-55° to +125°C	Standard Mil
AT40KAL040KW1MMQ	-55° to +125°C	Mil Std 883 Level B

Package Drawing

Multilayer Quad Flat Pack (MQFP) 160-pin



	mm		mils	
	Min	Max	Min	Max
A	1.96	2.66	.077	.105
C	0.10	0.20	.004	.008
D	37.90	39.30	1.492	1.548
D1	26.90	27.50	1.059	1.083
E	37.90	39.30	1.492	1.548
E1	26.90	27.50	1.059	1.083
e	0.650 BSC		.0256 BSC	
f	0.25	0.35	.010	.014
A1	1.70	2.10	.067	.083
A2	0.10	0.30	.004	.012
L	5.50	5.90	.216	.232
N1	40		40	
N2	40		40	

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